Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

OK to be entered CP 3/15/06

Listing of Claims:

1. (Currently Amended) A memory card comprising an erasable and programmable nonvolatile memory and a control circuit,

wherein a memory ~~array~~ area of ~~said~~ the nonvolatile memory includes a plurality of erasing blocks and is adapted to store an erasing table for storing ~~a~~ first flags each of which indicates ~~indicating~~ whether ~~the memory area~~ a datum stored in a corresponding erasing block is ~~a vacant area~~ valid or ~~not in every erasing unit~~invalid,

wherein ~~said~~ the memory ~~array~~ area includes a plurality of memory cells that have a predetermined threshold voltage, and

wherein ~~said~~ the control circuit has pre-erasing control to ~~previously~~ erase ~~a predetermined memory area~~ the datum stored in an erasing block corresponding to a~~the~~ first flag which indicates that a datum is invalid, ~~indicating the vacant area~~ irrespective of an operation instruction from ~~the~~ outside for instructing an~~the~~ address for changing the threshold voltage of a memory cell.

2. (Currently Amended) The memory card according to claim 1,

wherein ~~a~~ the erasing table further includes second flags each to indicate ~~indicating~~ whether ~~the memory area~~ a corresponding erasing block, for which the corresponding first flag indicates an invalid datum, is ~~in the erase condition~~ already erased or not ~~corresponding to said first flag, indicating whether the memory area is a vacant area or not, is also included~~, and

wherein ~~said~~ the control circuit ~~regards, in the pre-erasing control, the memory area indicated to be a vacant area by said first flag and indicated to be a not yet erased area by said second flag, as an object area to be erased~~performs the pre-erasing control to erase a datum stored in the erasing block, for which the corresponding first flag indicates an invalid datum and the corresponding second flag indicates a datum which is not erased.

3. (Currently Amended) The memory card according to claim 2,

wherein ~~said~~ the erasing table comprises an area ~~having said~~ for storing the first flags and ~~said~~ the second flags.

4. (Currently Amended) The memory card according to claim 3,

wherein ~~said~~ the control circuit ~~alters, in the pre-erasing condition, the corresponding second flag to the condition indicating the erased area after completion of the~~

~~erasing process to the memory area as an erasing process object~~selects one erasing block having a datum indicated to be invalid by the first flag and a datum indicated to be not erased by the second flag, and erases the datum stored in the one erasing block, and then, changes the second flag corresponding to the one erasing block to indicate an erased condition.

5. (Currently Amended) The memory card according to claim 4,

wherein ~~said~~ the control circuit ~~performs the control to assign, to a new memory area for writing a new data to be updated, the memory area designated as a vacant area with said first flag and as an erased area with said second flag~~selects one erasing block having a datum indicated to be invalid by the first flag and a datum indicated to be erased by the second flag, and stores new datum to the one erasing block, and then changes the first flag corresponding to the one erasing block to indicate a valid condition.

6. (Currently Amended) The memory card according to claim 5,

wherein ~~said~~ the control circuit ~~updates the corresponding first flag of memory area to which an old data is written to the condition to indicate a vacant area after the data is written into said new memory area~~changes the first flag corresponding to another erasing block, in which a previous datum is stored, to an invalid condition and

changes the second flag corresponding to the another erasing block to a not erased condition.

7. (Currently Amended) The memory card according to claim 6,

wherein ~~said~~ the memory ~~array~~ area ~~of nonvolatile memory~~ further comprises an address translation table indicating ~~the correspondence between~~ a logical address and a physical address ~~of memory area~~corresponding to the logical address, and

wherein ~~said~~ the control circuit ~~updates, after the data is written to said new memory area assigned on the basis of said first and second flags, said address translation table through correspondence between the physical address of memory area to which the data is written and the logical address before the update of the corresponding first flag to the condition to indicate a vacant area~~changes the physical address from the another erasing block, in which the pervious datum had been stored, to the one erasing block, in which the new datum has been stored, after storing the new datum to the one erasing block and before changing the first flag corresponding to the another erasing block to the invalid condition.

8. (Currently Amended) The memory card according to claim 1,

wherein ~~said~~ the control circuit executes ~~said~~ the pre-erasing control in response to the power-on of the memory card.

9. (Currently Amended) The memory card according to claim 1, further comprising a cipher arithmetic processing circuit,

wherein ~~said~~ the control circuit executes ~~said~~ the pre-erasing control in parallel to the cipher arithmetic process executed with ~~said~~ the cipher arithmetic processing circuit in response to a predetermined security command.

10. (Currently Amended) The memory card according to claim 1,

wherein ~~said~~ the control circuit executes ~~said~~ the pre-erasing control in response to a predetermined exclusive command.

11. (Currently Amended) The memory card according to claim 1,

wherein ~~said~~ the control circuit starts ~~said~~ the pre-erasing control in response to the completion of a command process.

12. (Currently Amended) The memory card according to claim 11,

wherein when an instruction by another command is issued before or after the start of the erasing operation by ~~said~~ the pre-erasing control, the process of the relevant command is executed preferentially.

Claims 13 - 20 (cancelled)